Reewaj Adhikari

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Computer Engineering student with hands-on experience in embedded systems, RTL and structural Verilog design, FPGA synthesis, and arithmetic datapath architecture. Skilled in FSM-based control, microcontroller programming, networking, and Linux-based system validation using simulation and timing analysis tools. Seeking a hardware and embedded engineering internship focused on processor architecture, FPGA design, server systems, and hardware validation.

Education

North Carolina State University Raleigh, NC
Bachelor of Science in Computer Engineering May 2027

Skills & Interests

Programming & RTL: Verilog, C, C++, Python, MATLAB, Bash
Digital & Hardware Design: FSMs, datapath/control separation, timing analysis, ADC/DAC, PWM, SPI, UART, I²C
FPGA & Tools: Vivado, LTspice, KiCad, Oscilloscope, Logic Analyzer, Git
Technical Interests: Processor architecture, FPGA design, hardware validation, server and system-level infrastructure

Relevant Coursework

Embedded Systems Design (ECE 306): MSP430 programming, ADC/DAC, GPIO, UART, PWM, real-time systems
Systems Design and Digital Hardware (ECE 310): Verilog, FSMs, datapaths, FPGA synthesis and timing analysis
Computer Networking (ECE 407): TCP/IP, routing protocols, transport mechanisms, data center networking

Experience

Zebra Robotics Raleigh, NC
Technical Systems Intern Jan. 2025 – Aug. 2025

- Engineered a network-attached storage (NAS) system for 20,000+ users, improving reliability and data access efficiency by 40%.
- Configured and validated Windows and Linux workstation environments with secure remote access.
- Automated setup scripts, user accounts, and diagnostics, reducing onboarding and lab prep time by 30%.

IEEE at NC State Raleigh, NC
Web Developer Aug. 2024 – Present

- Redesigned and maintained IEEE's website, improving event signup efficiency by 25% and overall engagement.
- Implemented interactive features using JavaScript, React, and Node.js, enhancing usability across devices.
- Collaborated with team to develop dashboards and optimize system performance for students and faculty.

Projects

Serial BCD Arithmetic Logic Unit | *Verilog RTL, FSM Design, FPGA Synthesis*

- Designed a fully serial BCD ALU with dual finite state machines for packetized streaming input and output control.
- Implemented 9's complement subtraction and BCD correction logic (+6 adjustment).
- Designed 41-bit SIPO input framing and 28-bit PISO output serialization datapath for continuous streaming operation.
- Verified functionality using custom testbench and waveform analysis.
- Performed FPGA synthesis and reviewed post-synthesis timing and resource utilization reports.

Autonomous Wi-Fi-Controlled Car | *C, Assembly, RTOS, TI Microcontrollers*

- Developed RTOS-based firmware on TI microcontrollers for deterministic task scheduling and sensor fusion.
- Integrated PWM motor control, line-following, and obstacle detection sensors with safety routines.
- Enabled wireless control and telemetry via IoT Wi-Fi module for remote monitoring and navigation.
- Debugged timing and communication issues across motor, sensor, and wireless subsystems using hardware tools.